



Errata Sheet

MM32F0010

Rev 1.3

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1 Overview

This Errata Sheet describes all known functional issues for the MM32F0010 series products, aiming to provide users with errata information and corresponding solutions for these products.

Table1 Applicable Series Models

Series	Model
MM32F0010	Please refer to the MM32F0010 Series Data Sheet for the latest model list

2 Summary

Table 2 Errata Sheet Summary

Functional Module	Brief Description	Ver C	Ver D	Ver F	Detailed Description
TIM	TIM Single-Edge Trigger Encoder Counting Anomaly	x	x	-	错误!未找到引用源。
ADC	ADC Multi-Channel Conversion Window Compare Function Anomaly	x	x	x	错误!未找到引用源。
Flash	Programs Executed in SRAM Cannot Perform Page Erase, Programming, or Read Operations on Main Flash After Read Protection is Enabled	x	x	-	3.3.1
Flash	Cannot Read UID via SWD After Read Protection is Enabled	x	x	-	3.3.2
Low-Power Modes	Occasional Wake-Up Anomaly from Low-Power Modes Under Non-Specified Timing	x	x	x	3.4.1
SPI	SPI Slave Mode MISO Does Not Enter High-Z State When NSS is High	x	x	x	3.5.1

In the Version column, the letters indicate the chip version numbers where the phenomenon occurs. Chip version number information can be found in the chip marking. For specific details, please refer to Section 2.2 "Marking Information" in the MM32F0010 Series Data Sheet.

3 Issues and Solutions

3.1 TIM

3.1.1 TIM Single-Edge Trigger Encoder Counting Anomaly

Issue:

In TIM encoder mode, the TIMx_SMCR register's SMS bits can be configured to count on TI1 edges, TI2 edges, or both TI1 and TI2 edges simultaneously. Regardless of the counting method configured, counting pulses and direction signals are generated based on the transition sequence of the two input signals, and the counter counts up or down accordingly, while the hardware sets or clears the TIMx_CR1 register's DIR bit correspondingly.

When SMS = 011 is set, the counter counts on both TI1 and TI2 edges. The DIR bit can be set or cleared based on the transition sequence of the two input signals, and the counter counts up or down accordingly.

When SMS = 001 or SMS = 010 is set, the counter counts on TI1 edges or TI2 edges respectively. The DIR bit can be set or cleared based on the transition sequence of the two input signals, but the counter only counts up and does not count down.

Solution:

None.

3.2 ADC

3.2.1 ADC Multi-Channel Conversion Window Compare Function Anomaly

Issue:

The ADC's window compare mode allows software to select the monitored channel via the CMPCH bits. When the converted value of the channel selected by CMPCH falls within the set window comparison range (CPMHDATA, CPMLDATA), the ADWIF bit in the status register ADSTA is set to 1.

It was found that when the ADC enables only one channel for conversion, the ADWIF bit in the ADSTA register is set or cleared based on the comparison between the converted value of the channel selected by CMPCH and the set window compare range values.

When the ADC enables multiple channels for conversion, the ADWIF bit in the ADSTA register is not set or cleared based on the comparison between the converted value of the channel selected by CMPCH and the set window compare range values. Instead, it is set or cleared based on the comparison between the converted value of the channel preceding the one selected by CMPCH in the conversion sequence and the set window compare

range values.

Solution:

When enabling only a single ADC channel for conversion, set the CMPCH bits to select the same channel as the actual monitored channel. When enabling multiple ADC channels for conversion, software must set the CMPCH bits to select the channel immediately preceding the actual monitored channel in the conversion sequence.

Example: ADC enables channels 1, 3, 4, and 5 for conversion, and enables channel 4 for window compare function.

Reference pseudo code:

```
// Initialize ADC
ADCInit();
// Enable channels 1, 3, 4, 5 for conversion
ADCChannelConfig(Channel_1|Channel_3|Channel_4|Channel_5);
// Set ADC window compare high and low thresholds
ADCAnalogWatchdogThresholdsConfig(Thresholds_High, Thresholds_Low);
// Configure window compare channel as Channel 3 (effectively monitors Channel 4)
ADCAnalogWatchdogChannelConfig(Channel_3);
// Enable ADC window compare function
ADCAnalogWatchdogCmd(ENABLE);
```

3.3 Flash

3.3.1 Programs Executed in SRAM Cannot Perform Page Erase, Programming, or Read Operations on Main Flash After Read Protection is Enabled

Issue:

After chip read protection is enabled, programs executed in SRAM cannot perform page erase, programming, or read operations on the Main Flash. Chip erase operations are not affected.

Solution:

In scenarios where read protection is enabled, programs performing page erase, programming, or read operations on the Main Flash must be placed and executed in the Main Flash memory area.

3.3.2 UID Cannot Read UID via SWD After Read Protection is Enabled

Issue:

When chip read protection is enabled, the chip's UID cannot be read via the SWD interface.

Solution:

To read the chip UID via SWD, the chip's read protection must be disabled first. .

3.4 Low-Power Modes

3.4.1 Occasional Wake-Up Anomaly from Low-Power Modes Under Non-Specified Timing

Issue:

With Flash prefetch enabled, or with non-wakeup source interrupts enabled, during the process of entering or waking from a low-power mode, there is a very small probability that the chip may execute incorrectly, leading to wake-up failure or abnormal behavior after wake-up.

Solution:

Before entering a low-power mode, disable Flash prefetch and disable non-wakeup source interrupts.

Use the latest version of the MM32F0010 Library Functions and Examples (version 1.2 or higher, $\geq$ LibSamples_MM32F0010_V1.2), and call the sleep/wakeup functions provided (PWR_EnterSTOPMode, PWR_EnterSTANDBYMode).

If the sleep/wakeup functions (PWR_EnterSTOPMode, PWR_EnterSTANDBYMode) are not used, code must be written strictly following the sequence of operations in these wakeup functions.

3.5 SPI

3.5.1 SPI Slave Mode MISO Does Not Enter High-Z State When NSS is High

Issue:

In SPI slave mode, the MISO pin does not support entering a high-impedance (High-Z) state when NSS is at a high logic level.

Solution:

When NSS is high, the program must configure the MISO pin to input mode.

4 Revision History

Table 3 Revision History

Date	Version	Content
2025/3/25	1.3	Added errata information "SPI Slave Mode MISO Does Not Enter High-Z State When NSS is High"
2025/3/18	1.2	Added errata information "Occasional Wake-Up Anomaly from Low-Power Modes Under Non-Specified Timing"
2023/2/23	1.1	Added "Programs Executed in SRAM Cannot Perform Page Erase, Programming, or Read Operations on Main Flash After Read Protection is Enabled" and "Cannot Read UID via SWD After Read Protection is Enabled"
2021/1/5	1.0	Initial creation of Errata Sheet